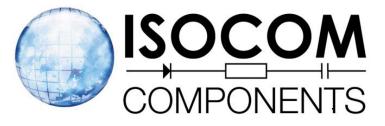
# **ICPL-3120**

### 2.5A Output Current, High CME Gate Drive Optocoupler

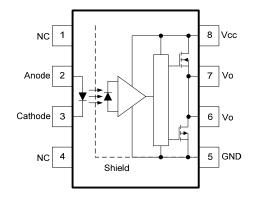


#### Description

The ICPL3120 optocoupler is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications and inverters in power supply system. It contains a AIGaAs LED optically coupled to an integrated circuit with a power output stage. The 2.5A peak output current is capable of directly driving most IGBTs with ratings up to 1200 V/100 A. For IGBTs with higher ratings, the ICPL3120 series can be used to drive a discrete power stage which drives the IGBT gate.

The Optocoupler operational parameters are guaranteed over the temperature range from  $-40^{\circ}C \sim +110^{\circ}C$ .

#### **Functional Diagram**



### Features

- · 2.5 A maximum peak output current
- 25 kV/us minimum Common Mode Rejection (CMR) at VCM = 1500 V
- 3.8 mA maximum supply current (I<sub>CC</sub>)
- Under Voltage Lock-Out protection (UVLO) with hysteresis
- Wide operating range: 15 to 30 Volts (V<sub>CC</sub>)
- Guaranteed performance over temperature  $-40^{\circ}C \sim +110^{\circ}C$ .
- Offer low power dissipation with  $R_{ON} \le 1\Omega$
- Fast switching speed, 500ns max propagation delay
- Safety approval: UL, cUL, VDE (In process)

#### Application

- IGBT/MOSFET gate drive
- Uninterruptible power supply (UPS)
- Industrial Inverter
- Induction heating

#### Truth Table

LED	V <sub>cc</sub> -GND (Turn-ON, +ve going)	V <sub>cc</sub> -GND (Turn-OFF, -ve going)	Vo
OFF	0 - 30 V	0 - 30 V	Low
ON	0 – 11.5 V	0 – 10 V	Low
ON	11.5 - 13.5 V	10 - 12 V	Transition
ON	13.5 - 30 V	12 - 30 V	High

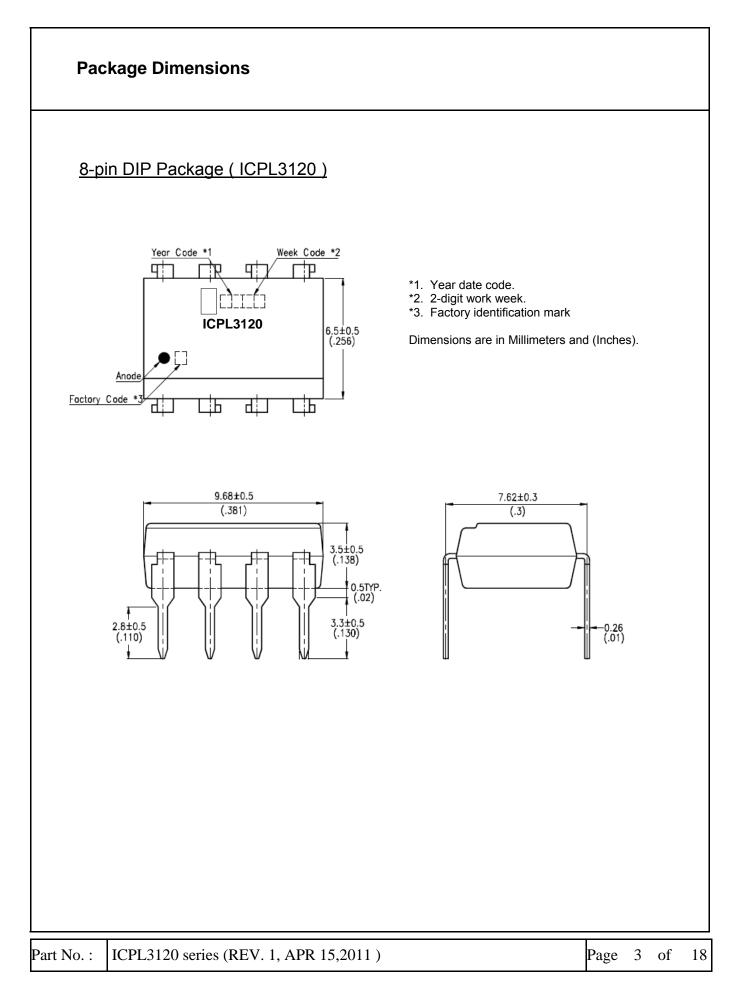
A 0.1µF bypass Capacitor must be connected between Pin 5 and 8. (Note 8)

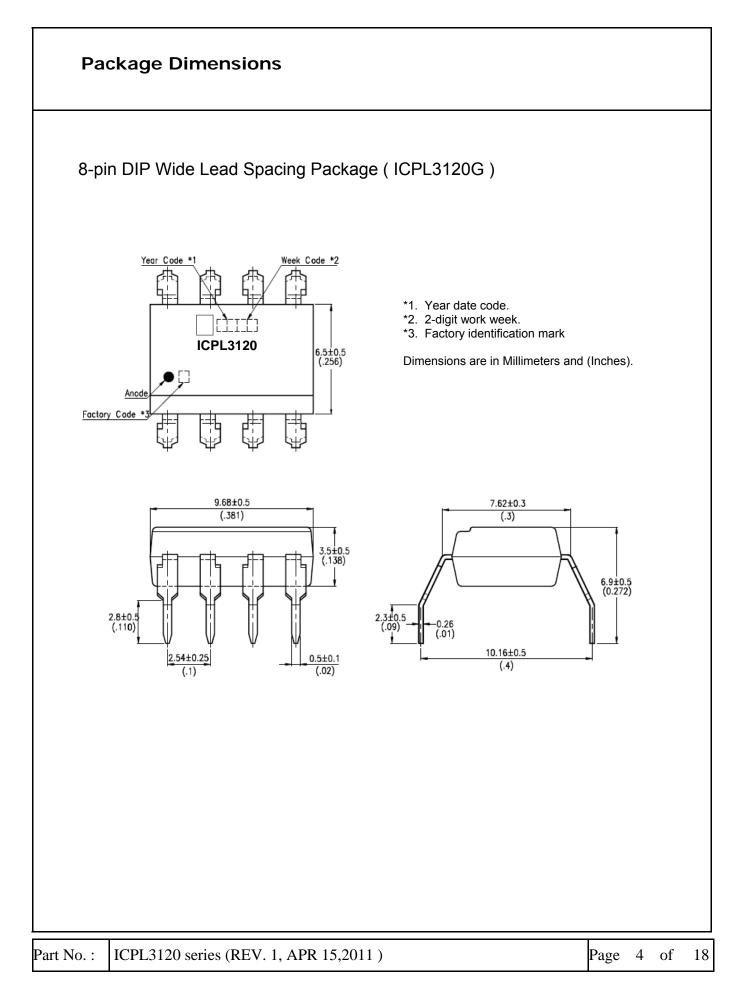
#### **ISOCOM COMPONENTS LTD**

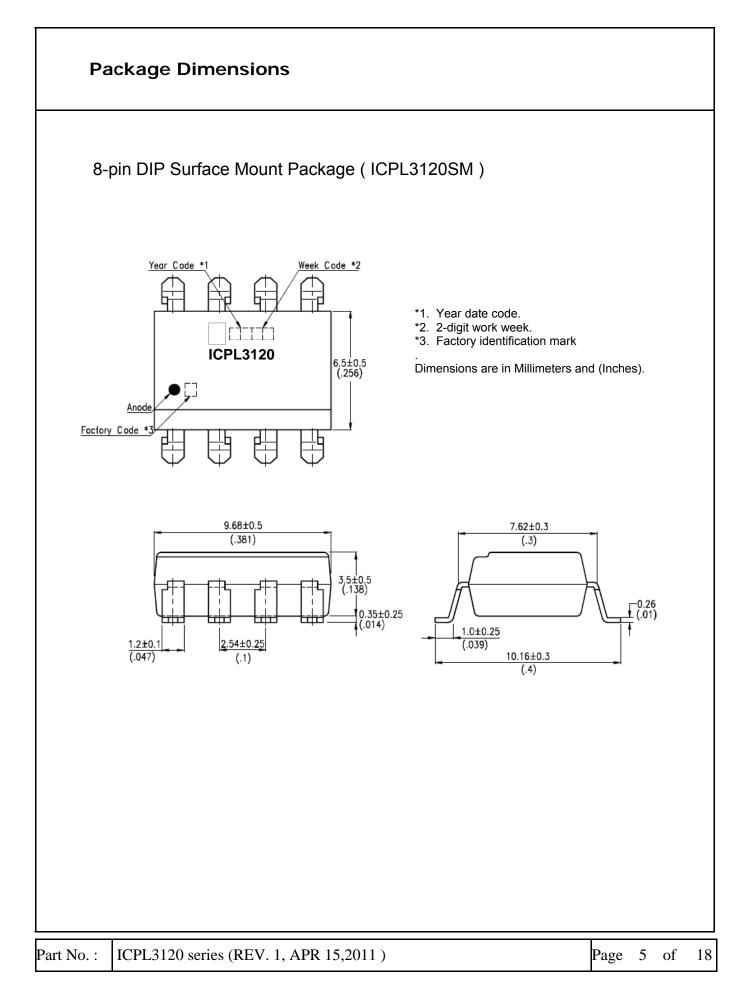
Unit 25B, Park View Road West, Park View Industrial Estate, Brenda Road Hartlepool, Cleveland, TS25 1YD Tel: (01429) 863609 Fax :(01429) 863581

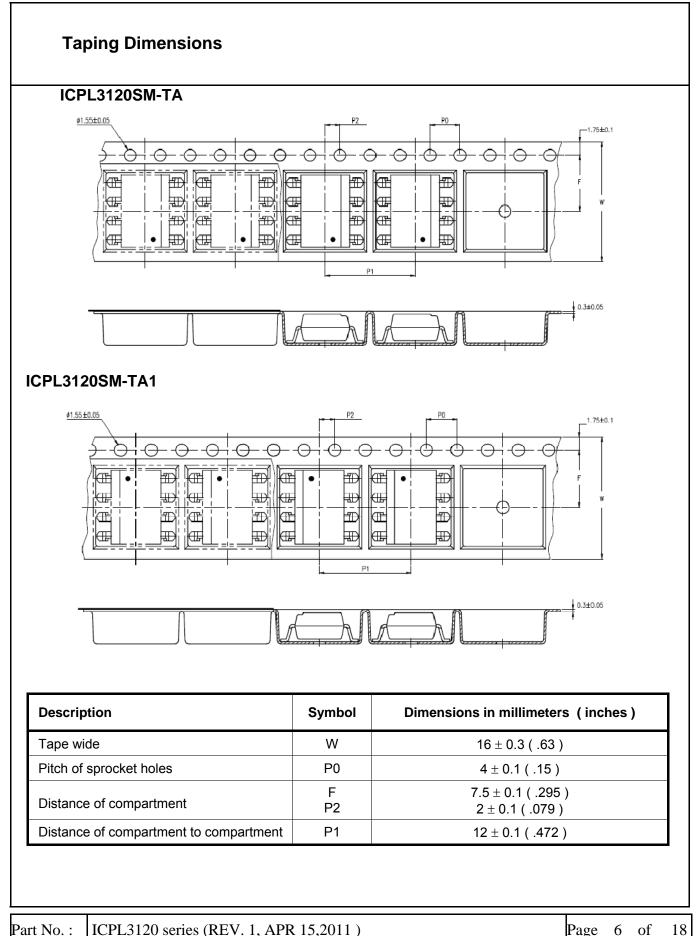
	Ordering Inf	ormatio	1
	Part	Option	Remarks
ľ			DIP-8
		G	Wide Lead Spacing, DIP-8
	ICPL3120	SM	Surface Mount, SMD-8
		T&R	Surface Mount, SMD-8, Pin 1 location at lower right of the reel
		T&R1	Surface Mount, SMD-8, Pin 1 location at upper left of the reel

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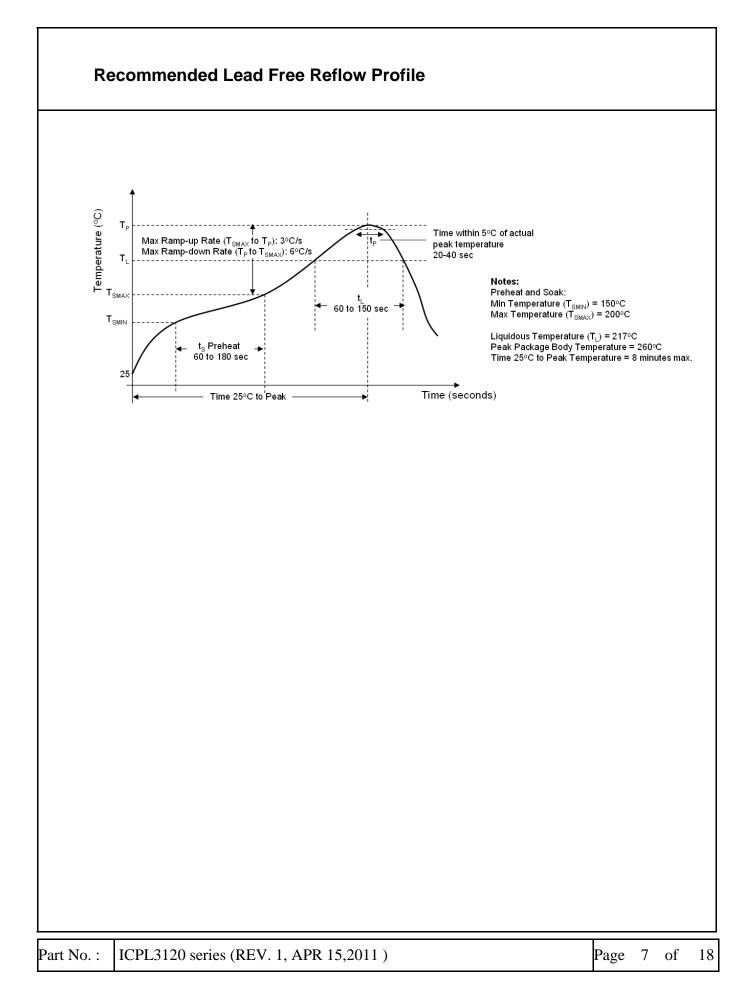








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#### **Absolute Maximum Ratings**

Ambient temperature = 25°C, unless otherwise specified. Stresses exceeding the absolute maximum ratings can cause permanent damage to the device. Exposure to absolute maximum ratings for long periods of time can adversely affect reliability.

Parameter	Symbol	Min	Max	Units
Storage Temperature	T <sub>ST</sub>	-55	125	°C
Operating Temperature	T <sub>A</sub>	-40	110	°C
Isolation Voltage	V <sub>ISO</sub>	5000		V <sub>RMS</sub>
Supply Voltage	V <sub>cc</sub>	0	35	V
Lead Solder Temperature <sup>(9)</sup>	T <sub>SOL</sub>		260	°C
Input				
Average Forward Input Current	I <sub>F(AVG)</sub>		25	mA
Reverse Input Voltage	V <sub>R</sub>		5	V
Peak Transient Input Current (<1 µs pulse width, 300 pps)	I <sub>F(TRAN)</sub>		1	А
Input Current (Rise/Fall Time)	t <sub>r(IN)</sub> /t <sub>f(IN)</sub>		500	ns
Input Power Dissipation (10)	Pi		45	mW
Output	·			
"High" Peak Output Current (1)	I <sub>OH(PEAK)</sub>		2.5	A
"Low" Peak Output Current <sup>(1)</sup>	I <sub>OL(PEAK)</sub>		2.5	Α
Output Voltage	Vo		V <sub>CC</sub>	V
Output Power Dissipation (11)	Po		250	mW
Total Power Dissipation	PT		295	mW

At least a 0.1uF or bigger bypass capacitor must be connected across pin 8 and pin
5. Failure to provide the bypass may impair the switching property.

- 9) 260°C for 10 seconds. Refer to Lead Free Reflow Profile
- 10) Derating Linearly above 70°C free-air temperature at a rate of -0.47 mW/°C
- 11) Derating Linearly above 70°C free-air temperature at a rate of 4.8mW/°C

### **Recommended Operating Conditions**

Parameter	Symbol	Min	Max	Units
Operating Temperature	T <sub>A</sub>	-40	110	°C
Supply Voltage	V <sub>cc</sub>	15	30	V
Input Current (ON)	I <sub>FL(ON)</sub>	7	16	mA
Input Voltage (OFF)	V <sub>F(OFF)</sub>	-3.0	0.8	V

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### **Electrical Specifications**

Parameters	Test Condition	Symbol	Min	Тур	Мах	Units	Figure
Input							
Input Forward Voltage	I <sub>F</sub> = 10mA	V <sub>F</sub>	1.2	1.37	1.8	V	15
Input Forward Voltage Temperature Coefficient	I <sub>F</sub> = 10mA	ΔV <sub>F</sub> / ΔΤ		-1.237		mV/ <sup>o</sup> C	
Input Reverse Voltage	Ι <sub>R</sub> = 10μΑ	BV <sub>R</sub>	5			V	
Input Threshold Current (Low to High)	V <sub>O</sub> > 5V, I <sub>O</sub> = 0A	I <sub>FLH</sub>		2.89	5	mA	9,16,21
Input Threshold Voltage (High to Low)	V <sub>O</sub> < 5V, I <sub>O</sub> = 0A	$V_{FHL}$	0.8			V	
Input Capacitance	f = 1 MHz, V <sub>F</sub> = 0 V	C <sub>IN</sub>		33		pF	
Output				-			
High Level Supply Current	Output Open, I <sub>F</sub> = 7 to 16 mA	I <sub>CCH</sub>		1	3.0	mA	7,8
Low Level Supply Current	Output Open, V <sub>F</sub> = -3 to +0.8 V	I <sub>CCL</sub>		1	3.0	mA	7,8
High level output current <sup>(1)</sup>	V <sub>O</sub> = (V <sub>CC</sub> - 6 V)	I <sub>OH</sub>	-2.0			А	2,3,19
Low level output current <sup>(1)</sup>	V <sub>O</sub> = (V <sub>EE</sub> + 6 V)	I <sub>OL</sub>	2.0			А	5,6,20
High level output voltage	I <sub>F</sub> = 10mA, I <sub>O</sub> = -100mA	V <sub>OH</sub>	V <sub>CC -</sub> 0.25	V <sub>CC -</sub> 0.1		V	1,3,17
Low level output voltage	I <sub>F</sub> = 0mA, I <sub>O</sub> = 100mA	V <sub>OL</sub>		V <sub>EE +</sub> 0.1	V <sub>EE +</sub> 0.25	V	4,6,18
UVLO Threshold	$V_{\rm O}$ > 5V, I <sub>F</sub> = 10 mA	V <sub>UVLO+</sub>	11.5		13.5	V	
	$V_{\rm O}$ < 5V, I <sub>F</sub> = 10 mA	V <sub>UVLO-</sub>	10	11.5	12	V	22
UVLO Hysteresis		UVLO <sub>HYS</sub>		1.6		V	

### **Switching Specifications**

Parameter	Test Condition	Symbol	Min	Тур	Max	Units	Figure
Propagation Delay Time to High Output Level	I <sub>F</sub> = 7 to 16 mA, Rg = 10 Ω, Cg = 10 nF,	T <sub>PLH</sub>	0.1	0.28	0.5	μs	
Propagation Delay Time to Low Output Level	f = 10 kHz, Duty Cycle = 50%	T <sub>PHL</sub>	0.1	0.31	0.5	μs	10,11, 12,13,
Pulse Width Distortion (7)		PWD			0.1	μs	14,23
Propagation delay difference between any two parts or channels <sup>(4)</sup>		PDD	-0.30		0.30	μs	
Output Rise Time (10 to 90%)		Tr		0.1		μs	22
Output Fall Time (90 to 10%)		Tf		0.1		μs	23
UVLO turn on delay	I <sub>F</sub> = 10 mA, V <sub>O</sub> > 5 V	T <sub>UVLO ON</sub>		1.5		μs	
UVLO turn off delay	I <sub>F</sub> = 10 mA, V <sub>O</sub> < 5 V	T <sub>UVLO OFF</sub>		0.2		μs	
Common mode transient immunity at high level output <sup>(5)</sup>	$I_F = 10 \text{ to } 16 \text{ mA},$ $V_{CM} = 1500 \text{ V},$ $TA = 25^{\circ}\text{C},$ $V_{CC} = 30 \text{ V}$	СМН	25	35		kV/µs	24
Common mode transient immunity at low level output <sup>(6)</sup>	$V_{F} = 0 V,$ $V_{CM} = 1500 V,$ $TA = 25^{\circ}C,$ $V_{CC} = 30 V$	CML	25	35		kV/µs	24

Specified over recommended operating conditions.

All Typical values at TA = 25°C and V $_{\rm CC}$  = 30 V, unless otherwise specified.

### **Isolation Characteristics**

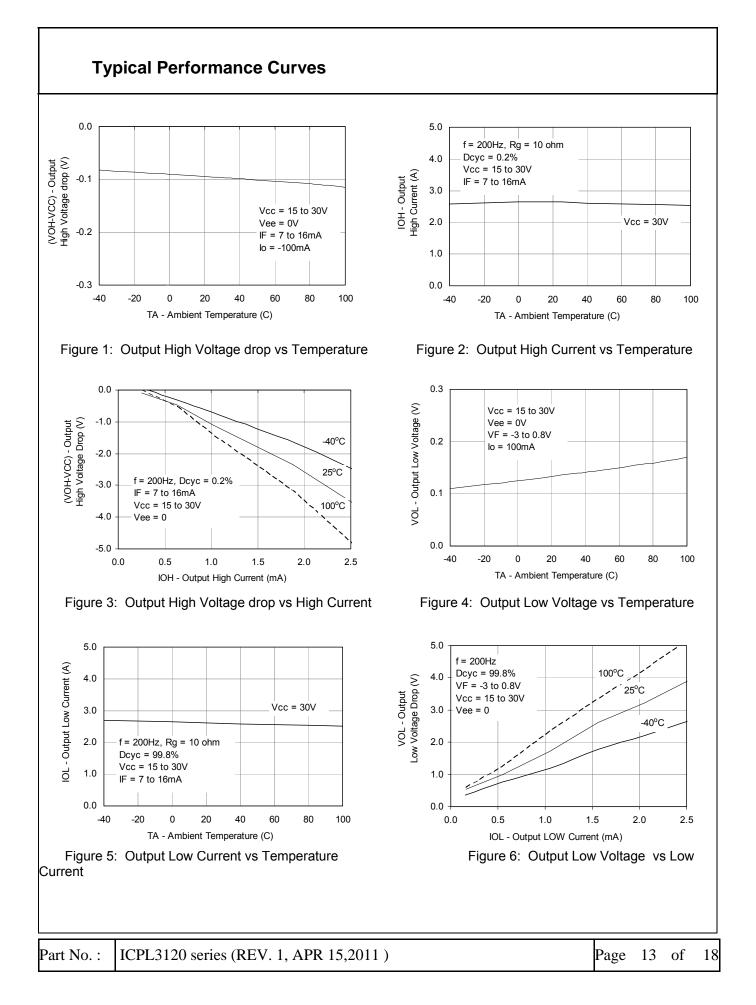
Parameter	Test Condition	Symbol	Min	Тур	Max	Units
Withstand Insulation Test Voltage <sup>(2) (3)</sup>	RH ≤ 40-60%, t = 1min, T <sub>A</sub> = 25°C	V <sub>ISO</sub>	5000			V
Input-Output Resistance <sup>(2)</sup>	V <sub>I-O</sub> = 500V DC	R <sub>I-O</sub>		10 <sup>12</sup>		Ω
Input-Output Capacitance <sup>(2)</sup>	f = 1MHz, T <sub>A</sub> = 25°C	C <sub>I-O</sub>		0.92		pF

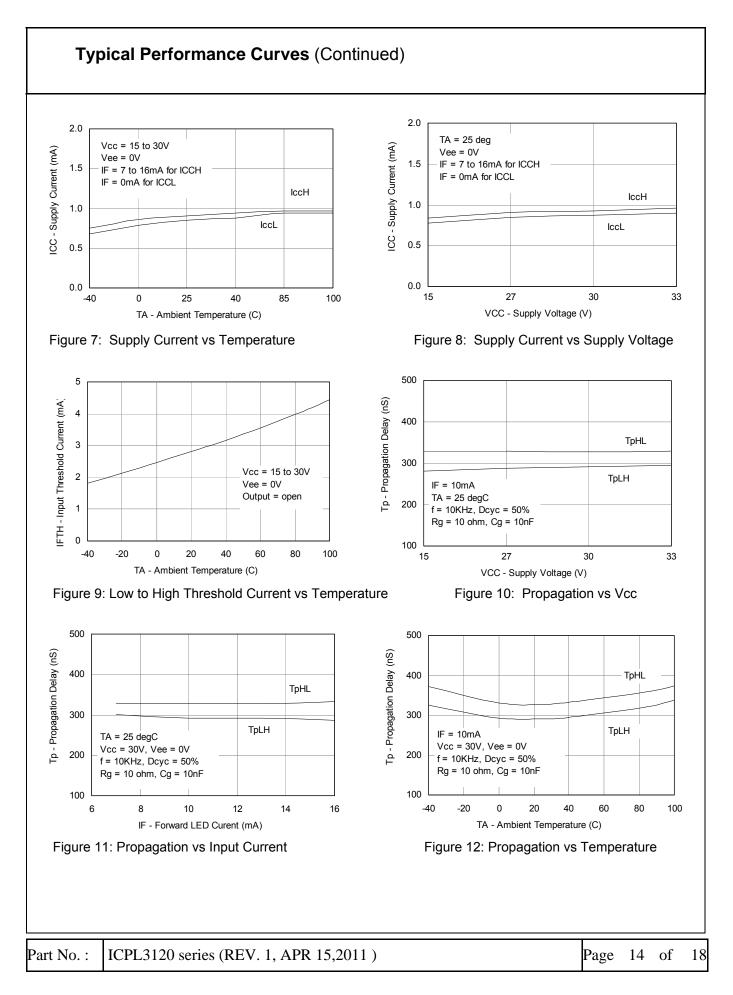
#### Notes:

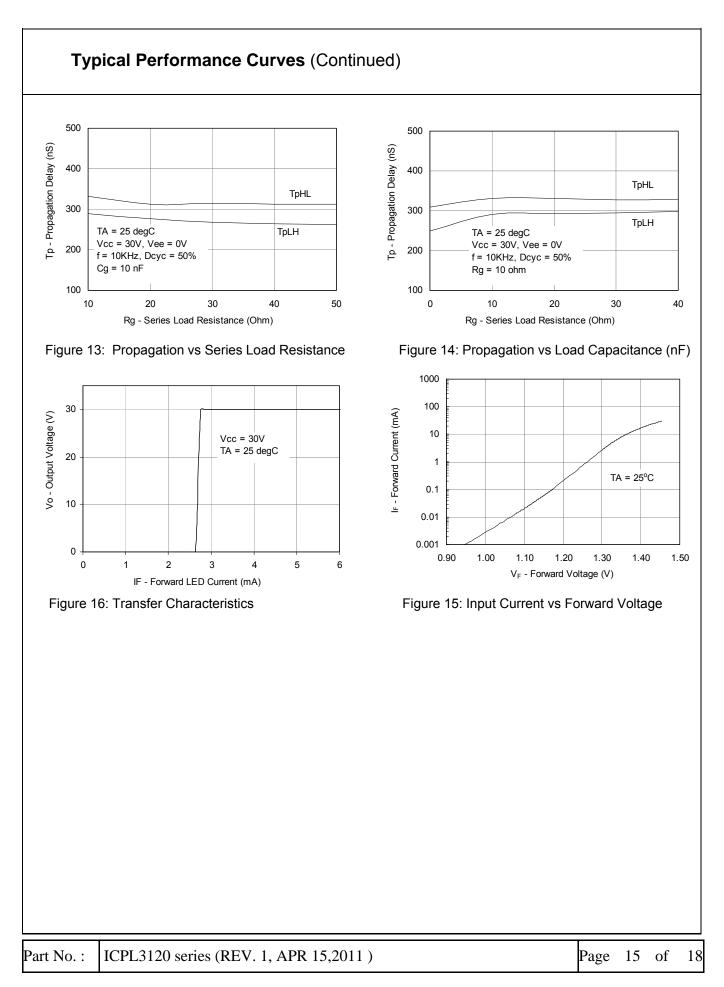
- 1) Maximum pulse width = 10us, maximum duty cycle = 0.2%.
- 2) Device is considered a two terminal device: pins 1, 2, 3 and 4 are shorted together and pins 5, 6, 7 and 8 are shorted together.
- 3) According to UL1577, each optocoupler is tested by applying an insulation test voltage  $\geq$  6000 Vrms for 1 second (leakage detection current limit,  $I_{I-O} \leq 6$  uA).
- The difference between T<sub>PHL</sub> and T<sub>PLH</sub> between any two ICPL3120 parts under same test conditions.
- 5) Common mode transient immunity in high stage is the maximum tolerable negative dVcm/dt on the trailing edge of the common mode impulse signal, Vcm, to assure that the output will remain high.
- 6) Common mode transient immunity in low stage is the maximum tolerable positive dVcm/dt on the leading edge of the common mode impulse signal, Vcm, to assure that the output will remain low.
- 7) Pulse Width Distortion is defined as  $|T_{PHL} T_{PLH}|$  for any given device.

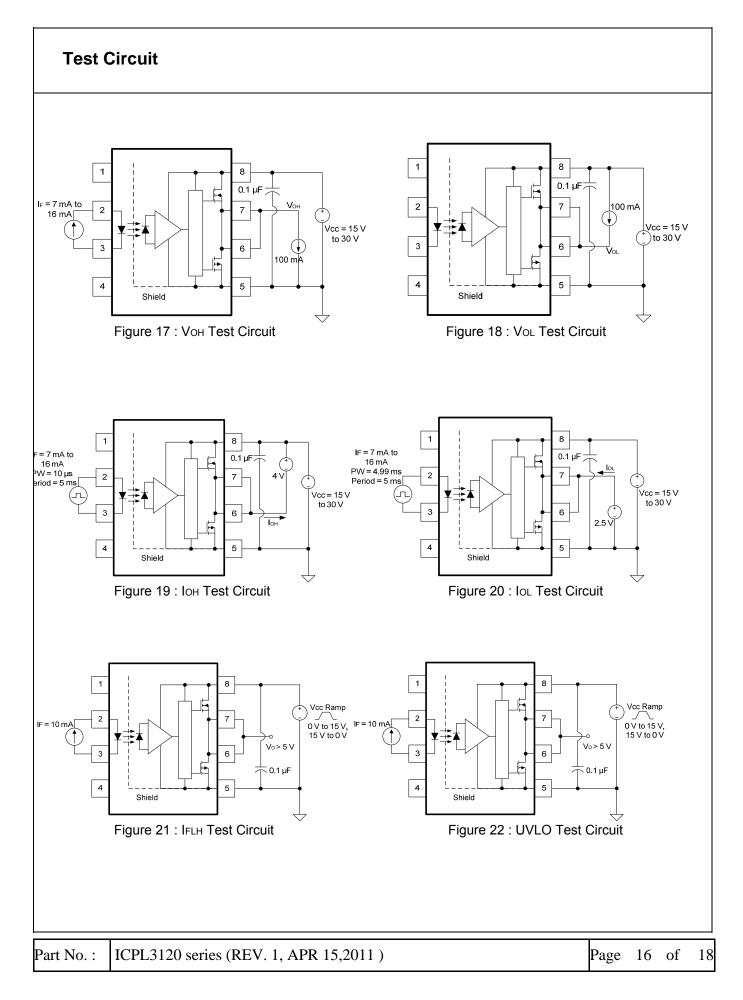
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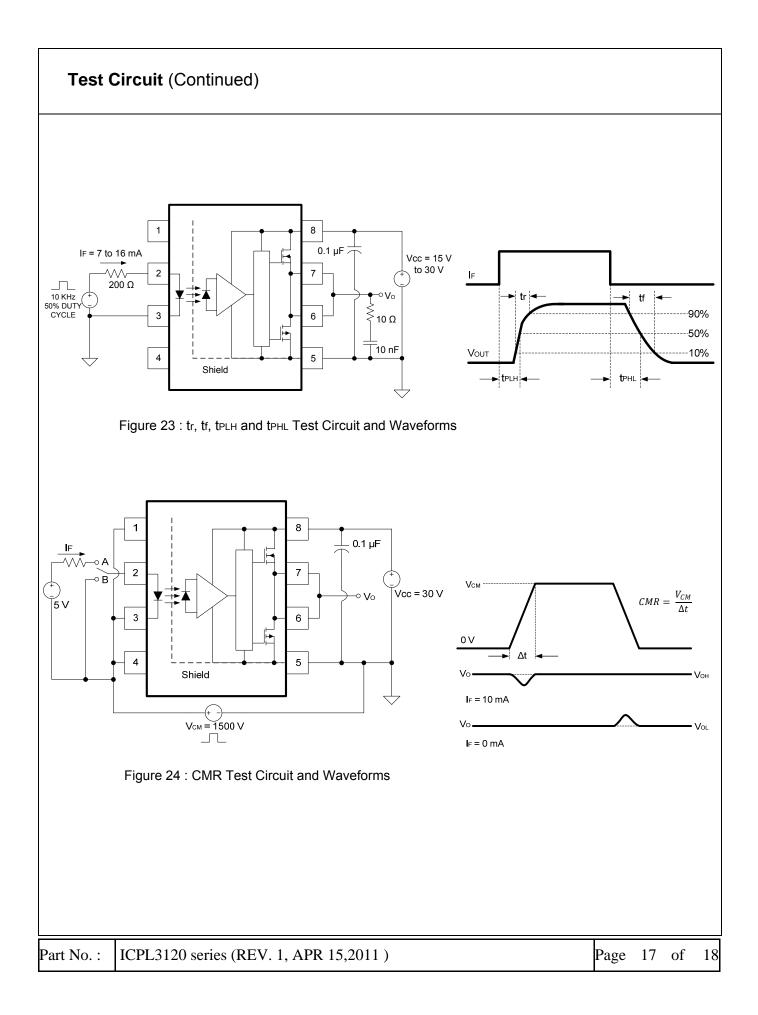
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#### Notice

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